IN THE CLAIMS

Please amend the claims as shown in the following detailed claim listing. The detailed claim listing is intended to reflect the amendment of previously pending claims 1, 3, 4, 6, 21, and 27. The specific amendments to individual claims are detailed in the following detailed claim listing.

1. (Currently Amended) A current reference comprising:

a current mirror circuit to force a first current to be substantially equal to a second current;

a control transistor coupled to the current mirror circuit to receive the first current, the control transistor having first and second biasing terminals across which a biasing voltage can be applied; ~~and~~

a variable resistor coupled between the first and second biasing terminals of the control transistor and coupled to the current mirror to receive the second current ~~.~~ ;and

a control loop to influence the biasing voltage.

2. (Original) The current reference of claim 1 wherein the variable resistor comprises a plurality of resistive devices in parallel, each of the plurality of resistive devices having a control input node to enable the resistive device.

3. (Currently Amended) The current reference of claim 1 ~~further comprising a control loop circuit to influence~~ wherein the variable resistor includes a plurality of resistive devices having binary weighted values.

4. (Currently Amended) The current reference of claim ~~3~~ 1 wherein the variable resistor comprises a plurality of resistive devices in parallel, each of the plurality of resistive devices having a control input node to enable the resistive device.

5. (Original) The current reference of claim 4 wherein the control loop circuit includes output nodes, and wherein the control input node of each resistive device is coupled to one of the output nodes of the control loop circuit.

6. (Currently Amended) A current reference comprising:

a current mirror circuit to force a first current to be substantially equal to a second current;

a control transistor coupled to the current mirror circuit to receive the first current, the control transistor having first and second biasing terminals across which a biasing voltage can be applied;

a variable resistor coupled between the first and second biasing terminals of the control transistor and coupled to the current mirror to receive the second current; and

a control loop circuit to influence the variable resistor, wherein the variable resistor comprises a plurality of resistive devices in parallel, each of the plurality of resistive devices having a control input node to enable the resistive device, ~~The current reference of claim 4~~ wherein the control loop circuit comprises:

a comparator to compare two voltages, the comparator having an output node; and

a state machine coupled to the output node of the comparator, the state machine having output nodes coupled to the control input nodes of the plurality of resistive devices.

7. (Original) The current reference of claim 1 wherein the control transistor comprises a NFET, and the first and second biasing terminals are a gate source of the NFET.

8. (Original) The current reference of claim 7 further comprising a second NFET having a drain terminal coupled to receive the second current from the current mirror, and having a source terminal coupled to provide the second current to the variable resistor.

9. (Original) The current reference of claim 1 further comprising a transistor coupled drain-to-source between the current mirror and the variable resistor.

10. (Original) An integrated circuit comprising:

a first current reference having a first current mirror with first and second current paths, a first control transistor coupled in the first current path, and a first variable resistor coupled in the

second current path and across biasing terminals of the first control transistor, the first current reference having an output node with substantially constant current;

a second current reference having a second current mirror with third and fourth current paths, a second control transistor coupled in the third current path, and a second variable resistor coupled in the fourth current path and across biasing terminals of the second control transistor; and

a control loop circuit having an input node coupled to an output node of the second current reference, and having an output node to influence the first and second variable resistors.

11. (Original) The integrated circuit of claim 10 further comprising a voltage reference having an output node coupled to a second input node of the control loop circuit.

12. (Original) The integrated circuit of claim 11 wherein the control loop circuit comprises a comparator responsive to the second current reference and the voltage reference.

13. (Original) The integrated circuit of claim 12 wherein the control loop circuit further comprises a state machine to influence the first and second variable resistors responsive to the comparator.

14. (Original) The integrated circuit of claim 12 further comprising an output node coupled to the output node of the second current reference to drive a resistor external to the integrated circuit, and an input node coupled to the comparator to sample an external voltage on the external resistor.

15. (Original) The integrated circuit of claim 10 wherein the first current mirror comprises two PFET devices.

16. (Original) The integrated circuit of claim 10 wherein the first variable resistor includes a first plurality of resistive devices in parallel, each of the first plurality of resistive devices including an NFET and an n-well resistor.

17. (Original) The integrated circuit of claim 16 wherein the second variable resistor includes a second plurality of resistive devices in parallel, each of the second plurality of resistive devices including an NFET and an n-well resistor.

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18. (Original) The integrated circuit of claim 17 wherein the control loop circuit is coupled to a gate of the NFET in each of the second plurality of resistive devices.

19. (Original) The integrated circuit of claim 18 wherein the first and second control transistors are NFET devices.

20. (Original) The integrated circuit of claim 10 wherein the first current reference further comprises a transistor coupled in the second current path between the first current mirror and the first variable resistor.

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21. (Currently Amended) A current reference comprising:

~~a control transistor having a gate terminal and a source terminal;~~

a variable resistor coupled across the gate terminal and source terminal of the control transistor, the variable resistor coupled to receive a generated current; and

a control loop circuit responsive to a ~~copy of~~ current equal to the generated current, the control loop circuit coupled to influence the generated current.

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22. (Original) The current reference of claim 21 further comprising a current mirror coupled to the control transistor and the variable resistor.

23. (Original) The current reference of claim 22 wherein the variable resistor comprises a plurality of variable resistance devices coupled in parallel, each of the plurality of variable resistance devices including an NFET responsive to the control loop circuit.

24. (Original) The current reference of claim 22 wherein the control loop circuit comprises a comparator responsive to an output node of the current mirror.

Cont A8

25. (Original) The current reference of claim 24 wherein the control loop circuit comprises a state machine responsive to the comparator to influence the variable resistor.

26. (Original) The current reference of claim 22 further comprising a transistor to support a variable voltage between the current mirror and the variable resistor.

A9

27. (Currently Amended) An integrated circuit comprising:

a control transistor coupled in a first leg of a current reference circuit, the control transistor having first and second biasing terminals;

a variable resistor coupled in a second leg of the current reference circuit and between the first and second biasing terminals of the control transistor; and

a control loop circuit to modify a resistance value of the variable resistor, the control loop circuit comprising a variable impedance output driver.

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28. (Original) The integrated circuit of claim 27 wherein the control loop circuit further comprises:

a comparator coupled to an output node of the variable impedance output driver; and

a state machine responsive to the comparator.

29. (Original) The integrated circuit of claim 28 wherein the variable resistor comprises a plurality of variable resistance devices coupled in parallel, each of the plurality of variable resistance devices including an NFET responsive to the state machine.

30. (Original) The integrated circuit of claim 27 further comprising an output node responsive to the variable impedance output driver to drive a resistor external to the integrated circuit, and an input node to sample an external voltage on the external resistor, and wherein the control loop circuit comprises:

a voltage comparator to compare the external voltage and an internal voltage; and

a state machine responsive to the voltage comparator to influence the variable resistor.